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PAPER

Microdroplet-based universal logic gates by electrorheological fluid

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We demonstrate a uniquely designed microfluid logic gate with universal functionality, which is capable of conducting all 16 logic operations in one chip, with different input voltage combinations. A kind of smart colloid, giant electrorheological (GER) fluid, functions as the translation media among fluidic, electronic and mechanic information, providing us with the capability of performing large integrations either on-chip or off-chip, while the on-chip hybrid circuit is formed by the interconnection of the electric components and fluidic channels, where the individual microdroplets travelling in a channel represents a bit. The universal logic gate reveals the possibilities of achieving a large-scale microfluidic processor with more complexity for on-chip processing for biological, chemical as well as computational experiments.

Introduction

During the last decade, microfluidics, which is a low-cost fast-diagnosis and micro-synthesis technique, has become a mainstay of Point-of-Care (POC) and Lab-on-a-Chip (LOC) applications.^{1–3} In microfluidic research, individual manipulation of microdroplets is an exciting challenge.^{4–6} Those pico-litre droplets are perfectly suitable for micro-synthesis, drug screening, and chemical tracing.^{7–11} As a result, large-scale integration and high-density control unions^{12–14} are required.^{6,14}

Compared with off-chip macro-scaled solenoid arrays, controlled by peripheral equipment, on-chip control components have spurred interest and attracted enormous attention owing to their scalability and cascability. Among the proposed on-chip control schemes, the electrowetting-on-dielectric (EWOD) system^{15,16} is good for the fine “digital” control of droplets, yet its pre-defined round-trip control, reflecting its “electronic” rather than “fluidic” nature, diminishes its flexibility. On the other hand, simple control schemes are required while preserving the delicacy of micro-devices.^{17,18} Droplets need to be “smart” enough to “think” for themselves, meaning that outputs should fully depend on inputs in assigned tasks. Researchers have

demonstrated this possibility by both kinetic stream regulation^{19,20} and static geographical bubble/droplets manipulation.^{21,22} In digital microfluidics, droplets are used as miniature reactors, and are also good equivalents of binary 1 and 0. Moreover, the colour, volume and components of the droplets extend the context of “information” to dimensions other than the binary 0/1.

In our previous work, we successfully achieved a simple on-chip logic function IF and NOT,²³ in which a droplet can indeed “think” logically. Here we report a more delicate design, the first microfluid universal logic device, where all 16 Boolean logic operations (according to two inputs) can be realized: operating functions are defined only by the power supply. Giant electrorheological fluid (GERF), introduced as the computing media, translates fluidic information into electronic and mechanic information, back and forth, making this microfluid universal logic gate fully compatible with electronic devices. Since the universal logic gate is the most basic component of digitalized computing, this invention promises to become the building block of microfluidic processors. For example, it could be used in microfluidic computing¹⁷ and automatical reagent-adding in multi-step chemical reactions, such as multi-layer microsphere synthesis.

Principle

The critical material used for universal logic gates, giant electrorheological fluid (GERF), is a kind of “smart” colloid and its viscosity can be tuned by an applied electric field. The GER powder consisting of the nanoparticles coated with urea (BaTiO (C₂O₄)₂ + NH₂CONH₂), is mixed with sunflower oil with a weight concentration of 30%. A sufficiently strong electric field can even solidify GERF, and once the electric field is removed,

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the reverse process, liquefaction, occurs. This colloid, with its quick response time (within a few milliseconds) and very high yield stress (more than 300 kPa at a field strength of 5kv mm^{-1}),²⁴ is an ideal control-medium candidate for us in microfluidic chips with electric-field-assisted logic functionalities.

First-generation GERF components, like valves, digitalized GERF control, storage and display have already been realized in PDMS-based microchips,^{25–27} where, with the help of specifically designed electrodes embedded in the microfluidic channel, voltage input is utilized as the control signal for GERF reversible liquid–solid phase transition. We had further extended the context of “inputs” to droplet switches—conductive/high-dielectric droplets carried in insulate fluid. This, alterable impedance in fluidic form, is utilized to adjust the voltage applied to GERF, that is, as an “ON/OFF” switch of GERF’s phase change. In this work, we take the concept one step further: droplet trains in two or more separate channels can be electrically correlated to influence the GERF behavior, which is a perfect start for imitating a universal logic gate. In other words, by connecting microfluidic channels with chip-embedded conducting wires, fluidic communication and logic ‘thinking’ can be easily carried out.

Our designed configuration is illustrated in Fig. 1. As shown in Fig. 1(a), four individual DC power supplies are connected to conducting pads 1, 2, 5 and 6. The fluid channels and pads are electrically connected *via* the conducting strips (Ag–PDMS composite). With two additive capacitances (top, near pad 1&2), GERF’s voltage share is greatly diversified under different input combinations. To effectively share voltage applied to the GERF output channel, we intently composed the additive capacitances by GERF channels so they had the same width and electrode sizes as the controlled GERF channels, thus the impedances of all three GERF channels have equal constants Z_E . Accordingly, if the left signal channel is defined as channel A, and the right one B, the voltage applied to the GERF (central channel) is

$$V_{GERF} = |V_A - V_B| = f(V_1, V_2, V_3, V_4, Z_A(x_A), Z_B(x_B)), \quad (1)$$

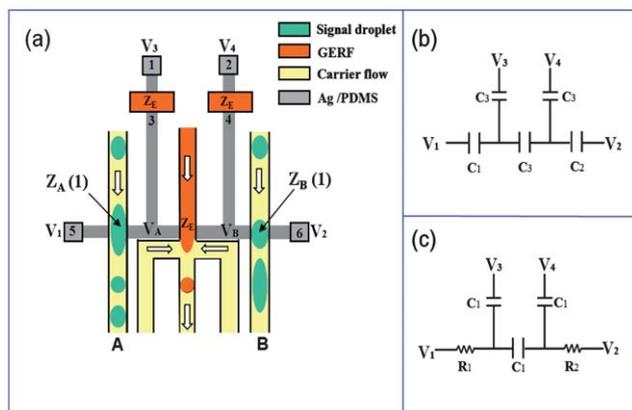


Fig. 1 (a) Working principle of the logic gate. 1–6 are the electrodes, Z_A and Z_B are the impedances from signal channels A and B, while $Z_A(1)/Z_B(1)$ indicates the signal droplet present between the electrodes, and Z_E is the GER fluid impedance; (b) equivalent circuit for dielectric fluids; (c) equivalent circuit for conductive signal fluids.

where $V_1 \sim V_4$ are the voltages applied to pads 5, 6, 1, 2; V_A and V_B are the electric potentials on either side of the output GERF channel; and $Z_A(x_A)$ and $Z_B(x_B)$ are the impedances provided by signal channels A and B, respectively. $x_i = 1$ ($i = A$ or $i = B$) indicates that a desired droplet is presenting between the signal electrodes, and $x_i = 0$, the carrier fluid flows only. Thereby, as x switches the electric pathway, we can arrange the values of V_1 , V_2 , V_3 and V_4 to preset a variable voltage V_{GERF} , so that only under a desired combination of $Z_A(x_A)$ and $Z_B(x_B)$ is the V_{GERF} equal to or higher than the critical voltage to solidify GERF. The equivalent circuits are shown in Fig. 1(b) and 1(c). When the fluids in the signal channels are dielectric characters, they can be considered as capacitance (Fig. 1(b)), while conductive ones could be viewed as resistances (Fig. 1(c)).

In following report, we will take a more intuitive example: if the signals are saturate KCl droplets carried by silicone oil, the conductive KCl droplets become trigger signals/switches (we could assume that $R_{KCl} \sim 0 \Omega$ and $R_{oil} \sim \infty$). This is because the conducting KCl droplet between two parallel electrodes is able to generate an electrical connection between the two electrodes, where an equal potential can be achieved. In this particular case, the voltage applied to the GERF (central channel) is

$$V_{GERF} = f(x_A, x_B) = \begin{cases} f(0, 0) = \frac{1}{3}|V_4 - V_3| \\ f(0, 1) = \frac{1}{2}|V_3 - V_2| \\ f(1, 0) = \frac{1}{2}|V_4 - V_1| \\ f(1, 1) = \frac{1}{2}|V_1 - V_2| \end{cases} \quad (2)$$

The principle of voltage arrangement methodology could be illustrated by this concise example: assuming V_C to be the critical GERF solidification, we can set a V_0 that $\frac{2}{3} V_C > V_0 \geq \frac{1}{2} V_C$, and the corresponding input voltage combination for 16 possible logic functions are listed in Table 1. Take the logic function of ‘A OR B’ as an example: we set $V_1 = V_2 = 0V$, $V_3 = -V_4 = 3V_0$, thus when $Z_A = Z_A(0) = R_{oil}$, $Z_B = Z_B(0) = R_{oil}$, voltage on GERF is calculated as $V_{GERF} = 2V_0 \geq V_C$; when $Z_A = Z_A(1) = R_{KCl}$, $Z_B = Z_B(1) = R_{KCl}$, we could get $V_{GERF} = 0V$; when $Z_A = Z_A(0) = R_{oil}$, $Z_B = Z_B(1) = R_{KCl}$ or $Z_A = Z_A(1) = R_{KCl}$, $Z_B = Z_B(0) = R_{oil}$, it is $V_{GERF} = 1.5V_0 < V_C$. It means that only when both the area between electrodes of two signal channel are filled with oil, the GERF will be stop, otherwise the GERF will flow out continuously. In another word, if there is signal droplet in either A or B, the GERF could flow out, which is the logic function of OR.

Actually, to achieve the same function, one could have many different combinations of the supplied voltage. Table 1 just lists one possible solution. For example, we could also set $V_1 = -V_2 = V_0$ and $V_3 = -V_4 = 3V_0$ to achieve logic function ‘A AND B’, where the GERF solidifies only when signal droplets $Z_A(1)$ and $Z_B(1)$ present together, which is shown in the Fig. 1(a). What’s more, in other cases, either in capacitance model or resistance model or even more complex ones, we could calculate all the voltage needed according to the equivalent circuits.

Results

The real configuration of the microfluid universal logic gate is shown in Fig. 2. In the 3D illustration in Fig. 2(a), we can see

Table 1 Combinations of supplied voltages for all 16 possible logic functions with an input of 2 variables

Function	V_1	V_2	V_3	V_4
FALSE (Whatever A and B , the output is false)	$-3 V_0$	$3 V_0$	$3 V_0$	$3 V_0$
A AND B (Output is true if and only if both A and B are true.)	$0V$	$0V$	$4 V_0$	$-4 V_0$
$A \rightarrow B$ (A doesn't imply B . True if A but not B .)	$0V$	$4 V_0$	$4 V_0$	$-4 V_0$
$B \rightarrow A$ (B doesn't imply A . True if B but not A .)	$4 V_0$	$0V$	$-4 V_0$	$4 V_0$
IF A (True whenever A is true.)	$3 V_0$	$3 V_0$	$3 V_0$	$-3 V_0$
IF B (True whenever B is true.)	$3 V_0$	$3 V_0$	$-3 V_0$	$3 V_0$
A XOR B (True if A is not equal to B .)	$3 V_0$	$-3 V_0$	$-3 V_0$	$3 V_0$
A OR B (True if A is true, or B is true, or both.)	$0V$	$0V$	$3 V_0$	$-3 V_0$
A NOR B (True if neither A nor B .)	$4 V_0$	$-4 V_0$	$0V$	$0V$
A XNOR B (True if A is equal to B .)	$4 V_0$	$4 V_0$	$0V$	$0V$
NOT A (True if A is false.)	$0V$	$2 V_0$	$-2 V_0$	$0V$
NOT B (True if B is false.)	$2 V_0$	$0V$	$0V$	$-2 V_0$
$A \rightarrow B$ (A implies B . False if A but not B , otherwise true.)	$2 V_0$	$2 V_0$	$0V$	$-2 V_0$
$B \rightarrow A$ (B implies A . False if B but not A , otherwise true.)	$2 V_0$	$2 V_0$	$-2 V_0$	$0V$
A NAND B (A and B are not both true.)	V_0	$-V_0$	$0V$	$0V$
TRUE (Whatever A and B , the output is true.)	$0V$	$0V$	$0V$	$0V$

^a V_C is the critical voltage for fully solidification of GERF, and V_0 could be a value which fulfils $\frac{2}{3} V_C > V_0 \geq \frac{1}{2} V_C$

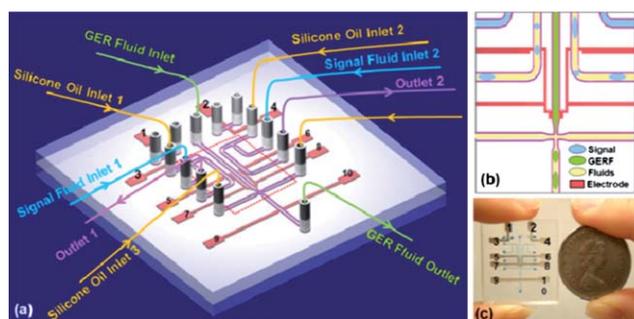


Fig. 2 (a) Structure of the universal logic gate; (b) close up view of key part in centre; (c) optical image of the universal logic gate chip.

seven fluid injection inlets: four for carrier fluid (silicone oil), two for signal fluid (saturate KCl solution) and one for GERF; with the three outlets including two for signal droplets and one for GERF droplets. Conducting pads, numbered from 1 to 10, are embedded for the voltage supply (pads 1, 2, 5, 6), internal connection (pads 3, 4, 7, 8) are reserved for droplet detection (pads 9, 10). The electrodes are connected by said pads and on-chip conducting wires, forming an on-chip signal passing way. The key portion of this configuration, outlined by the red dashed line, is enlarged in Fig. 2(b). The two streams of signal droplets (blue) generated at the T-junctions flow in two independent signal channels (A and B) on both sides. On the walls of each signal channel, there is a pair of parallel electrodes (signal electrodes). Connected to these, another pair (output electrodes) is positioned on the GERF (green) channel to control GERF droplet generation. Once the GERF is stopped by the responsive electric field, a GERF droplet will be generated at the adjacent flow-focusing junction. Fig. 2(c) is an optical image of the microfluidic chip, the size of which is compared with that of a Hong Kong dollar coin, and all the channels are filled with blue dyed DI water for better viewing.

The experimental testing results, as expected, show that all of the 16 Boolean logic operations can be effectively executed in this logic gate. As there are 4 combinations of input signals (droplet status presented in the electrodes) from A and B

channels, [(0, 0), (0, 1), (1, 0) and (1, 1)] for each logic operation, in total there were 64 experimental results. Four logic operations could be merged into their mirrored ones (such as $A \rightarrow B$ into $B \rightarrow A$ and IF B into IF A), thus there are 48 independent situations in total, which are all listed in Fig. 3. In these experiments, blue-dyed saturate KCl solution was employed as the signal fluid and silicone oil as the carrier fluid. Correspondingly, the resistance of the signal droplets was negligible compared with that of the carrier fluid. The GERF, appearing in a dark grey color, flowed in the middle channel, and its responsive droplet formation at the flow-focusing junction, is highlighted in red in the figure. The black pattern is the Ag/PDMS conducting component.²⁸ The detailed voltage arrangement for each logic function could refer to Table 1 and the truth table for each situation is inserted in the right upper corner of each image. In our experiment, the critical voltage for GERF solidification is tested to be around 250 V, so that V_0 is chosen to be 300 V. It is remarkable that the only difference among the arrangements for different functions is the four input voltages. And under the same configuration, the GERF droplet formation is relied on the input signal x_A and x_B .

Fig. 4 provides an example of how the XOR gate operation is realized. The GERF flow is depended on the combination of input signal A and B, as shown in Fig. 4(a–d), with the truth table inserted in the upper right corner. According to huge resistance difference between the droplet (KCl solution) and carrier fluid (silicone oil), the input droplet sequences both in channel A and B could be seen as switches (droplet – switch on, carrier fluid – switch off), equivalent circuit is shown in Fig. 4(e) and also in the right lower corner of each image for the different input situation (a)–(d). The necessary voltage to fully stop the GERF, as tested, was 300 V; accordingly the voltage inputs were approximately set as $V_2 = V_3 = -450 V$, $V_1 = V_4 = 450 V$. Thus, when $x_A = x_B = 1$, $V_{GERF} \sim 900 V$; when $x_A = x_B = 0$, $V_{GERF} \sim 300 V$; when $x_A = 1$, $x_B = 0$ or the reverse ($x_A = 0$, $x_B = 1$), $V_{GERF} \sim 0 V$. This means that if and only if $x_A = x_B$ (*i.e.* there is the same input at both signal electrode pairs), the GERF will stop flowing, and a yield output GERF droplet will be generated. The input signals A and B and output O in a same period of time were measured

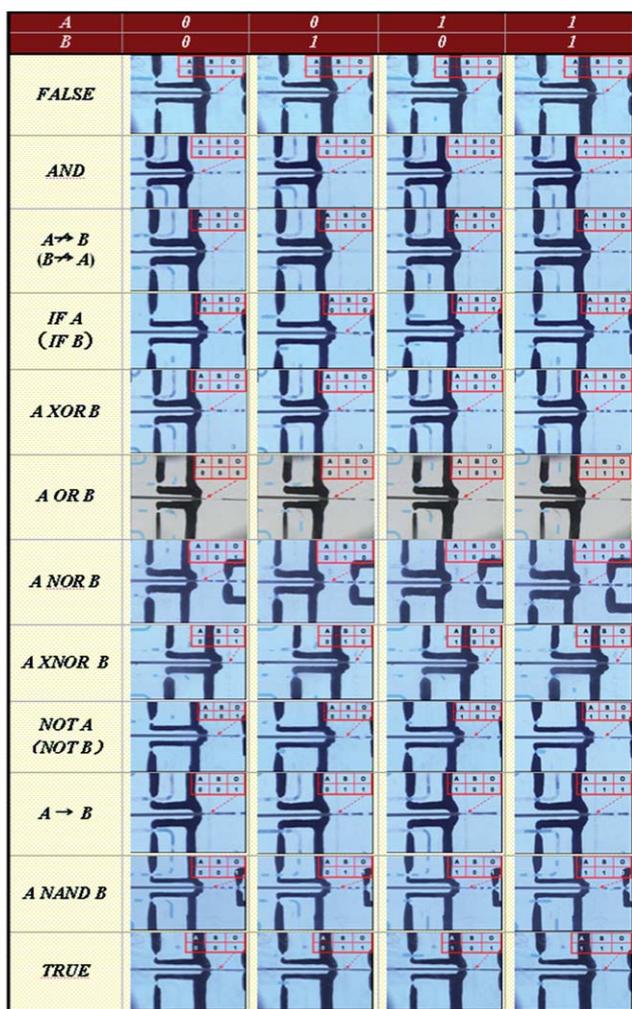


Fig. 3 Experimental results of all logic functions.

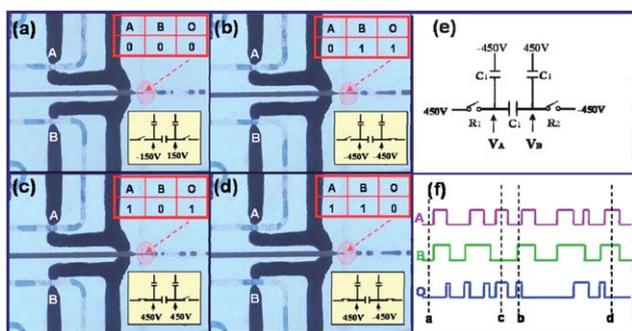


Fig. 4 (a–d) Optical images of results of XOR gate logic functions. The truth table and equivalent circuit is inserted in each picture. (e) Schematic view of equivalent circuit and voltage arrangement. (f) Comparison of two input signals and one output signal. The relevant positions of image (a–d) are marked.

according to captured video and compared in Fig. 4(f) for an intuitional illustration. This figure shows that the response of the output GER fluid is exactly depended on the combination of input signals, and the response time is quite short (ten to several hundred milliseconds).

Discussion

This microfluidic logic scheme requires, for alternation among logic functions, only rearrangement of input voltages, which is very convenient for function re-setting. Unlike electronic devices, traditional integrated microfluidic circuits are restricted, by their PDMS-based soft lithographic fabrication process, to pre-defined shapes. As our logic gate has a universal structure for deviated functions, its large-scale integration requires only structural repetition of identical units; system reprogramming, similarly, calls only for rearrangement of voltage inputs.

GERF functions in this device not only as fluidic logic output but also as an electronic information carrier and a mechanical pressure source to generate pressure for cascaded fluid control. Meanwhile, this device is compatible with a variety of GERF-based devices, such as demonstrated GERF-based mixer, storage, and displays. After an output GERF droplet is generated, it can be utilized to provide mechanical actuating/braking force, to control/generate a third stream of signal fluid, which is the key point in cascading for GERF-based computing schemes. Moreover, all these GERF-based microfluidic components have their chip-embedded electrodes, which can serve as information interfaces with electronic devices such as oscilloscopes or PCs. These electrodes can also function as connecting ports to electronic computing devices, meaning that reprogramming tasks can be achieved with the aid of PCs, if needed.

The generated GER droplets could be used as indicator of chronological order of the signal droplets, the control of downstream manipulation, such as droplet merging for chemical reactions, and when it is applied to the signal droplet generation part, it could also form a feedback control of generation of droplets consisting of different chemicals.

By using this device, communication between fluids could be realized without much peripheral equipment. Combined with other functions in microfluidic chips, multi-step reactions and biological testing in microfluidic chips would become automatic.

Experimental

Microfluidic chip fabrication

The master material of the chip mold used in these experiments were SU8-2050 (MicroChem Corp. 90 Oak St. Newton, MA, USA) and PR4903 (AZ Electronic Materials Hong Kong Limited, Unit 601-2, Li Po Chun Chambers, 189 Des Voeux Road Central, Sheung Wan, Hong Kong). Photolithography was utilized to fabricate chip masters with a height about 90 μm . The microfluidic chips were made of polydimethylsiloxane (PDMS) (Sylgard 184 silicone elastomer kit, Dow Corning Corporation, Midland, MI48686-0994, USA) and conducting component Ag-PDMS.²⁸ The PDMS gel is prepared by mixing base and curing agent in a ratio of 10 : 1, while the conducting component was composed of a mixture of PDMS gel and Ag particles (1.2–2.2 μm silver platelets, Unist Business Corp. Shanghai, China) with an Ag weight concentration of 86%. The fabrication method of Ag-PDMS conducting component embedded PDMS microfluidic chip could be found in ref. 28.

The fabrication process is shown in Fig. 5 and described as follows: (a) Master: the substrate glass wafer is cleaned with standard cleaning solution, e.g. $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1 : 1 : 5$

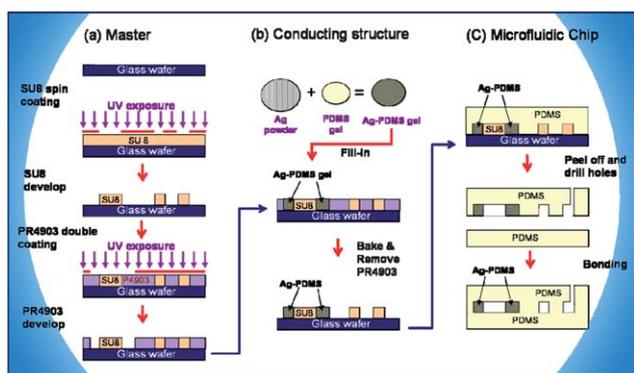


Fig. 5 The fabrication process of the microfluid universal logic gate.

(volume ratio). SU8-2050 is spin-coated with a thickness ~ 90 μm , and baked. After exposure, it is baked again and developed in a SU8 developer. PR4903 is then double coated on the substrate with SU8 pattern to derive the thickness of ~ 90 μm , baked, exposed and developed with a solution of (AZ400K : DI water = 1 : 3). (b) Conducting structures: PDMS base and curing agent is mixed at ratio of 10 : 1, and then mixed with Ag particles with an Ag weight concentration of 86%. The mixture is ground by a mortar for uniform dispersion. The mixture is filled into the groove of PR4903 and baked for full solidification. Then PR4903 could be removed by acetone and the substrate is cleaned by ethanol and DI water. (c) Microfluid chip: PDMS gel is prepared by mixing the base and curing agent in a ratio of 10 : 1. It is then degassed and poured onto the substrate with SU8 pattern and conducting structures. After solidification, PDMS slab is peeled off the substrate with channels and conducting structures embedded in, drilled inlets/outlets, and bonded with another flat piece of PDMS slab. Thus the electrode embedded PDMS microfluid chip fabrication is completed.

Equipment and chemicals

High voltage is supplied by Spellman SL300 (High Voltage Electronics Corporation, Hauppauge, NY11788, USA).

Silicone oil (100cSt, Clearco Products, 3430G Progress Drive, Bensalem, PA19020) Signal fluid: potassium hydroxide (KOH, from VWR International Ltd. Poole, BH15 1TD, England) is dissolved in DI water to form saturated solution at 23 $^{\circ}\text{C}$, and dyed blue.

Conclusions

In conclusion, we have presented a uniquely designed microfluid universal logic gate with the help of giant electrorheological fluid (GERF) as the working media. Our experiment shows that the fabrication is uncomplicated and the equipment required is quite simple. The configuration of on-chip electric circuit makes sure that all 16 logic operations could be achieved on one chip while arranging different voltage inputs. The results also demonstrate one of the logic operations, XOR gate. The results show that the output of GER droplets fully depends on the input signals. Although the GER droplet generation may have a little bit delay, the generated GER droplets could well present the relationship of two input signal droplets. This universal logic gate could be

brought into play in automatic microfluidic chemical reaction investigations, biological reactions and testing, drug screening, etc.

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